First Generation Mainframes

First Generation Mainframes:

The IBM 700 Series

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INTRODUCTION

THE IBM 700 SERIES

International Business Machines (IBM) Corporation was one of the first computer manufacturers to develop large computer systems. Its early computer systems – the 700 Series and the 7000 Series – introduced the "family" of computers concept although individual models could be incompatible with each other. In this case, the family concept was focused on a technology base for the central processors, a set of processes to manufacture computer systems repeatedly to the same set of specifications, reliability, and standards that allowed storage devices and unit record peripherals to be shared among the different models.

As Bashe, Johnson, Palmer and Pugh (1986) discussed in Chapter 2 – Electronic Calculation, IBM had developed considerable expertise in building electronic calculators. Several of these such as the SSEC and the Harvard Mark I, which I consider computer systems, were discussed in *Birthing the Computer: From Relays to Vacuum Tubes*. As computer systems concepts evolved during and immediately after World War II, it seemed logical that IBM extend these calculator concepts to develop computer systems.

The early history of IBM computing machines in the post-650 vacuum tube era comprised two families of mainframe computer systems – each with models having their own instruction sets and operating systems. These are:

IBM 70x family - the 1st generation mainframes
IBM 70xx family – the 2nd generation mainframes

By mainframes, we mean large computer systems – usually encompassing a large room – that comprised a central processing unit and its memory; high speed large storage peripherals such as magnetic tapes, drums and discs; and a variety of slow-speed unit record peripherals. The IBM 70x family was built using vacuum tubes for the CPU, but magnetic drums for the main memory. Figure I-1 depicts an IBM advertisement for its vacuum tubes. IBM followed the 70x family with the 2nd Generation

70xx family, which was based on magnetic cores and transistors. The IBM 7000 Series will be described and discussed in a future volume of this series.

Each of these machines contributed to the future development of IBM's unified system, the IBM System/360 Series and its successors. Architectural ideas developed for these machines are reflected today in the IBM zSeries computing systems. The IBM 360 and successors will be described and discussed in a future volume of this series.

This volume examines the IBM 700 Series computer systems – one of the first mainframe families - although different models had different instructions sets.

The IBM 70x/70xx computing machines were a computer systems family that presented five incompatible ways of storing data, but which were connected by a family label:

First Mainframe: IBM 701 (Defense Calculator) – 36 bits/18 bits
Scientific: 704, 709, 7090, 7094, 7040, 7042, 7044 – 36 bits
Commercial: 702, 705, 7080, 7010 – variable length character strings
Decimal: 7070, 7072, 7074 – 10 digit words
Scientific Supercomputer: 7030 (Stretch) – 64 bits

There were no systems labeled 707 or 708 and no systems labeled 7020, 7050 or 7060 as part of the 7xxx series. The IBM 703 was a one-of-kind special purpose machine delivered to the National Security Agency, but nothing else is known about this machine.

Figure I-1. IBM "Fingers" Advertisement
Source: IBM Corporation UNK
Courtesy of International Business Machines Corporation, © International Business Machines Corporation.

CHAPTER ONE

IBM 701

The IBM 70x computer family represented the first mainframe computer systems that IBM developed for commercial sale for scientific and business data processing use. The IBM 701 was created in 1951 when Thomas J. Watson Sr. approved James Birkenstock's proposal for a new computing machine using Cathode Ray Tube (CRT) memory with about 20,000 digits of memory per system, and with a clock cycle allowing it to multiply two numbers in one millisecond. As it was designed during the Korean War, in response to a request by the U. S. Department of Defense, it was known as the Defense Calculator. It was produced by a team led by J. A. Haddad and Nathan Rochester.

At that time there were about twenty digital computers operational around the world. Birkenstock believed that there might be a market for about thirty or more of these machines in the defense industry. The Defense Calculator was designed relatively quickly because IBM already had significant experience through both in-house and commercial products. The driving design philosophy was to keep the equipment simple and to a minimum, to make it fit a simple logical pattern, and to avoid special-purpose devices (Buchholz 1953).

IBM spent considerable time determining the physical characteristics of the IBM 701. As Werner Buchholz noted (Buchholz 1953):

> "The proper choice of word length, and hence, the number of parallel channels required in the computer, is a question which cannot be answered lightly. If the word length is too short, there will be many applications for which a single word is not enough to carry all the bits needed to represent a number…. Too great a word length is also bad. The time for carrying and shifting increases, and thus the speed goes down. The cost of the arithmetic circuits and registers and the cost for a given number of words of storage goes up."

Further, he stated:

> "Thus with a given set of applications there will be an optimum word length for which the speed is at a maximum or the cost is at a minimum. The relationship between these variables is, of course, far from simple, and a compromise is needed in any case."

In a succinct set of statements, Buchholz captured the primary design problem for at least two generations of computer architects. IBM conducted a survey of existing machines and applications, ultimately determining that a word length of between 10 and 12 digits or about 35 to 41 bits was desirable. Additionally, single address machines required at least 18 bits for storage of operation codes and addresses given a specified memory size. Since the secondary memory was magnetic tape, a tape technology study showed that 6 parallel channels for data storage were optimal. Thus, the word size should be a multiple of 6 bits so that subparts of the word could be stored in successive locations on tape. As a result, IBM arrived at 36 bits for the IBM 701 word size.

IBM President Thomas J. Watson announced the IBM 701 Electronic Data Processing System at an annual meeting on April 29, 1952. The name "Data Processing Machine" implied that it could process all types of data in different venues. The first production model was shipped to IBM's corporate headquarters at 590 Madison Avenue in New York in December 1952, where it became an instant favorite with sidewalk gawkers. In fact, it was installed in the same room that was previously occupied by IBM's SSEC. This IBM 701 was devoted to technical consulting operations for a variety of customers from industry and commerce. A dedicated team of IBM scientists was assigned to support the customer base in solving their problems.

The second machine, which had serial no. 1, was delivered to the Los Alamos Scientific Laboratory (LASL) in Los Alamos, New Mexico on April 1, 1953, and began working at the site within three days. It operated until the autumn of 1956. A second machine was installed at LASL in 1954. The electrostatic memory, which was "not too reliable", held 2048 36-bit words. The system consisted of the central processor unit, one card reader, one printer, one memory drum storage unit, two tape drives ("…which often did not work"), and one card punch (Lazarus, Voorhees, Wells, and Worlton 1978).

The Defense Calculator represented the first machine that could be produced in a sufficient quantity to satisfy the needs of a growing customer base and was a driving design principle for IBM (Buchholz 1953). Moreover, this modular machine had various detachable components that comprised the system and were capable of being detached from each other. This also marked the beginning of IBM's philosophy of building

machines that could be incrementally upgraded rather than replacing the whole system.

It was the first IBM machine in which programs were stored in an internal, addressable, electronic memory. An IBM 701 is depicted in Figure 1-1. Another view of an IBM 701 may be viewed at Columbia University's website: http://www.columbia.edu/cu/computinghistory/701.html. Additional photos of the IBM 701 and its components may be viewed at http://www-03.ibm.com/ibm/history/exhibits/701/701album.html. Other photos can be found at Bitsavers: http://bitsavers.informatik.uni-stuttgart.de/pdf/ibm/701/pictures/.

Figure 1-1. IBM 701 Electronic Data Processing Machine
Source: http://www-03.ibm.com/ibm/history/exhibits/701/701_intro.html
Courtesy of International Business Machines Corporation, © International Business Machines Corporation.

The IBM 701 was built as a binary, single address scientific computing machine and had a word size of 36 bits and an instruction set of 33 operations. An IBM 701 rented for around $16,000 per month (Columbia 2004a). Brown (1955) noted that at the end of 1954, 18 of these machines were installed and fully operational. Ultimately, only 19 of these machines

were built and delivered (Patrick 1987). A list of the IBM 701 customers can be viewed at http://www-03.ibm.com/ibm/history/exhibits/701/701 customers.html.

Figure 1-2 depicts Ronald Reagan and Herb Grosch standing in front of an IBM 701 at General Electric's computer room. Reagan was host of the Columbia Broadcasting System's (CBS) General Electric Theater (and, later, 40th President of the United States) (Columbia 2004b).

Figure 1-2. IBM 701 at General Electric, Evendale, Ohio
Source: Bell 1957

The IBM 701 Data Processing System's major characteristics are depicted in Table 1-1 (Weik 1961, Bashe et al 1986). The IBM 701 established the 36-bit word length used only in a few of its machines, but which strongly influenced the machines of several other manufacturers.

Table 1-1 IBM 701 Characteristics

Feature	Value
Internal Representation	Binary Fixed Point
#Bits/Word	36
#Instructions/Word	2
#Bits/Instruction	18
Instruction Type	One Address
# Instructions	33
CPU Technology	Vacuum Tubes
CPU Registers	Accumulator Multiplier-Quotient Register
Electrostatic storage capacity (tube)	2,048 words of 36 bits each
Magnetic drum capacity	4 drums, each 2048 words of 36 bits (later systems)
Magnetic tape capacity	More than 8 million digits
Addition and subtraction	Fixed Point: 60 microseconds
Multiplication and division	Fixed Point: 456 microseconds
Tape reading and writing speed	12,500 words per second
Drum reading and writing speed	8,000 digits per second
Printed output	150 lines per minute
Punched card input	150 cards per minute
Punched card output	100 cards per minute

The IBM 701 was a single-sequence machine, meaning it could perform only one operation at a time. Thus, if it was performing I/O that is all it could do until the data transfer was complete. It ran at about 0.15 MIPS.

Thomas J. Watson, Jr. (1914-1993)
Thomas J. Watson Jr. was born in Dayton, Ohio in 1914. His father, Watson Sr., had accepted a position as General Manager of C-T-R in YEAR. A rather controlling individual given to outbursts of temper, Watson Sr. had a strained relationship with his son. Watson Jr. graduated with a degree in from Brown University. He then became a salesman with IBM, but disliked working there because of the cult of personality that had developed around his father, the CEO. He joined the Air National Guard just before the U.S. entered World War II. By 1942, he was an aide to

Major General Follett Bradley, a position which ultimately helped to improve his self-confidence.

After the war, he returned to IBM to work for Charley Kirk, the Executive Vice President. When Kirk died in 1947, Watson, Jr. assumed many Kirk's responsibilities although not his title. However, in 1952, he was named President of IBM. Having becoming interested in computing in 1946 after visiting the Moore School to see ENIAC, Watson Jr. became a strong supporter of electronics and computing, and was responsible for developing IBM's computing businesses. He succeeded his father as IBM Chief Executive Officer in 1956.

He held many positions throughout his career, including the 11th National President of the Boy Scouts of America and the 16th Ambassador to the Soviet Union. He was awarded the Presidential Medal of Freedom by Lyndon Johnson in 1974.

1.1 IBM 701 SYSTEM CONFIGURATION

Source: IBM 1953c

A typical IBM 701 computer system consisted of eleven pieces of equipment: two magnetic tape units (each with two tape drives), a magnetic drum memory unit, a cathode-ray tube electrostatic storage unit (ESU) (a Williams Tube), an L-shaped arithmetic and control unit with an operator's panel, a card reader, a printer, a card punch and three power units (IBM Websites UNKc). Figure 1-3 depicts the IBM 701 system architecture.

The IBM 701 was very compact for its time. The logic was packaged in 64-pin modules with a row of 8 vacuum tubes on the front of each module. Its logical operations were performed by germanium diodes in the base of each module. Modules were plugged into a backplane. The backplane design permitted modules to be swapped while the system was powered up. IBM was an early innovator in the use of backplanes as a means of hosting different types of functional modules in its computer systems.

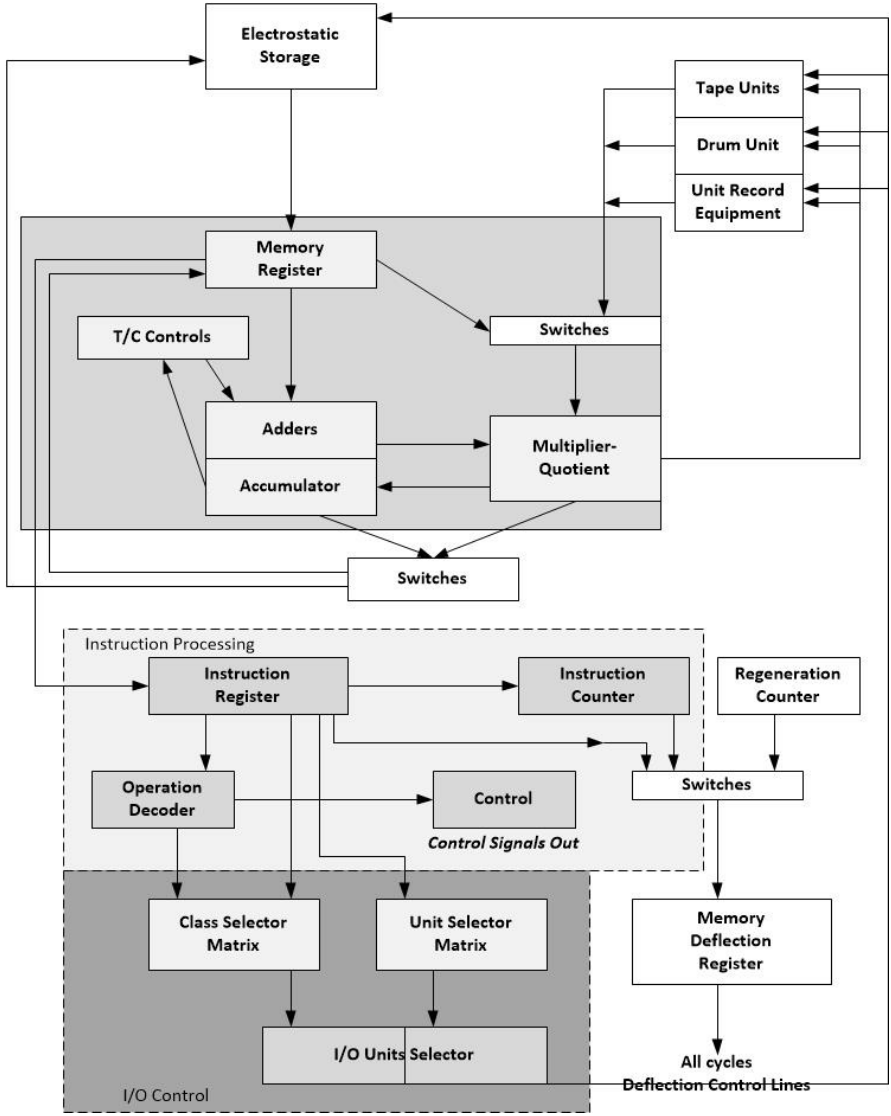

Figure 1-3. IBM 701 System Architecture
Source: Adapted from Frizzell 1953

1.1.1 701 ANALYTICAL CONTROL UNIT

The Analytical Control Unit (ACU) contained the arithmetic components, the input and output control circuitry, and the stored program control circuitry in a large cabinet. A separate cabinet housed the operator's console. The ACU also included the IBM 736 Power Frame #1, the IBM 741 Power Frame #2, and the IBM 746 Power Distribution Unit. These latter units supplied power to the rest of the components.

In addition, the ACU contained the timing and control circuits for the IBM 701. The IBM 701 had a pulse repetition rate of 1 megahertz. A 12-stage ring of trigger circuits generated twelve 1 microsecond pulses that constituted the basic machine cycle. This speed was driven largely by the regeneration requirements of the ESU.

1.1.2 701 REGISTERS

The Instruction Counter was a 12-bit counter that addressed 4096 half-words in memory. It was incremented by one at the end of each instruction. Even addresses specified the low-order 18 bits of a word while odd addresses specified the high-order 18 bits. The Instruction Counter could be modified by transfer instructions or skip instructions when the address portion of the Instruction Register was copied to the Instruction Counter.

The Memory Deflection Register controlled the addressing of the ESU. The Regeneration Counter contained the address of two words to be regenerated during the next cycle.

The principal elements of the arithmetic section were the Memory Register, the Accumulator, the MQ Register, the Binary Adders, and the True/Complement Controls. The Accumulator and the MQ register (Multiplier-Quotient Register) were coupled for long shifts, multiplication and division. The Memory Register was not directly accessible by the programmer. It served as the intermediate storage when moving data from the ESU into the ACU. The MQ register acted as the buffer in transferring data to and from the I/O devices. (Ross 1953).

Addition was performed at the rate of 60 microseconds per word, including the time to retrieve the instruction and the number and the necessary regeneration in the ESU. Multiplication was achieved by repeated adding and shifting, while division was performed by repeated subtraction and shifting. This avoided incorporating complex, expensive multiplication and division circuitry in the machine.

Every machine cycle included four types of regeneration: Instruction, Execution, Execution/Regeneration, and Regeneration. During an Instruction (I) cycle, an instruction was obtained from the ESU from the location specified by the Instruction Counter. The instruction was deposited in an internal Instruction Register, where it was interpreted by the decoding matrix.

During an Execution (E) cycle, the ESU was accessed at the address stored in the Instruction Register's address part. A number was read or written depending on the instruction. The instruction was executed during the Execution/Regeneration (E/R) cycle. One spot on the CRT was regenerated whose address was specified by the Regeneration Counter. During a Regeneration (R) cycle, one spot on the CRT was regenerated at the same time. Each of the 33 machine instructions was described by a pattern of these four cycles. For example an 'Add' instruction was specified by I, E, E/R followed by two R cycles.

1.1.3 706 ELECTROSTATIC STORAGE UNIT

The Electrostatic Storage Unit (ESU) contained a bank of 72 Cathode Ray Tubes (CRTs) that could store 10,240 digits equivalent to 2048 36-bit words with access time of about 12 microseconds. Data could be randomly accessed from the IBM 706 ESU. The cost per bit hovered around $1 – much less than vacuum-tube based flip-flop storage. The ESU rented for about $2600 per month.

The ESU regenerated memory in two ways. First, whenever memory was not being accessed, and second, through extra regeneration cycles added to each instruction. [Note: this approach is similar to garbage collection methods used in automatic memory management routines for programming languages a decade or so later.]

The memory capacity of 2048 words was deemed sufficient based on an application's size studied during a survey of applications. It included an allowance for subprograms that would replace circuitry for special functions. However, Buchholz believed that there would be little advantage in making the memory much larger than 2048 words. He noted that electrostatic storage was chosen because it represented a practical combination of high operating speed and adequate storage capacity.

1.1.4 I/O SYSTEM

Source: Stevens 1952

The I/O system implemented five functions for using an I/O device:

1. Selecting an I/O unit for reading, writing, or a control operation, such as rewinding a tape on a magnetic tape drive.
2. Interlocking the selected I/O unit's operation with the execution of a program.
3. Copying data to/from the electrostatic storage unit and the I/O units.
4. Synchronizing signals between the selected I/O unit and the CPU.
5. Disconnecting the I/O unit from control by the computer system its operation was completed.

Because the IBM 701 could continue to execute a program after it had selected an I/O unit, an interlock was implemented that "remembered" that the I/O unit had been selected for reading or writing. When the program encountered another select instruction, its execution was delayed until the operation on the previously selected I/O unit was completed. Information transferred to or from an I/O unit was always routed through the MQ register. These transfers occurred one word at a time and required the execution of a copy instruction on each transfer.

When a selected I/O unit was ready to transfer data, the program had to arrive at a copy instruction in order to perform the transfer. If no copy instruction was available, because the program had not reached the appropriate address, the I/O was disconnected from the computer and the interlock was turned off to prevent any information transfer.

1.1.5 736 MAGNETIC CORE STORAGE UNIT

The IBM 737 Magnetic Core Storage Unit (MCSU) replaced the ESU in 1956. The MCSU capacity was 4096 36-bit words and reduced the time for addition including access from 60 microseconds to 36 microseconds. It rented for about $6100 per month. An image of the IBM 737 may be viewed at http://www-03.ibm.com/ibm/history/exhibits/701/701_1415bx37.html.

1.1.6 IBM 716 PRINTER

The IBM 716 Line Printer printed up to 150 lines of alphanumeric characters or 180 lines of numbers per minute. Each line could contain up to 120 characters. This printer had 120 printing wheels that contained the 26 upper case letters, the numbers 0 to 9, and nine special characters and rented for approximately $800 per month. An image of an IBM 716 may be viewed at http://www-03.ibm.com/ibm/history/exhibits/701/7011415bx16.html.

1.1.7 IBM 731 MAGNETIC DRUM READER/RECORDER

The IBM 731 Magnetic Drum Reader/Recorder (MDRR) provided larger storage capacity but at a slower access speed. Each MDRR contained two drums divided into two logical drums each storing 2,048 words for a total capacity was 8192 words. The average time transfer time for one 36-bit word was about 1.28 milliseconds with an average access time of 50 milliseconds. It rented for about $1400 per month. The magnetic drum was a fixed-head device. A logical drum consisted of 36 tracks with 2048 storage cells around the periphery. It was clearly viewed as a swap space device and not for long term file storage.

The drum's linear density was 50 bits per inch. A drum timing track generated 2048 pulses used to locate the storage cells around the drum. To perform I/O, an instruction selected the logical drum. Then, a Set Drum Address instruction specified the storage cell to read or write. If no Set Drum Address instruction was executed, reading or writing began at cell 0. If a Copy instruction was given, 36 bits were transferred into the drum register. From there, the data was transferred to the MQ register.

1.1.8 IBM 753 MAGNETIC TAPE CONTROL UNIT/IBM 727 MAGNETIC TAPE UNIT

The IBM 753 Magnetic Tape Control Unit (MTCU) provided control circuitry for up to ten IBM 727 Magnetic Tape Units. It rented for about $2500 per month. The 727 Magnetic Tape Unit provided large capacity, intermediate speed storage, recorded data at 200 bits per linear inch. Data could be read or written at 15,000 characters per second. Each tape unit contained two reader/recorder units.

The magnetic tape was a half-inch wide 1,400-foot long non-metallic, oxide-coated band. A block of data recorded on the tape was called a

record. The amount of information recorded on a magnetic tape depended on the length of the records, but could approach 200,000 words.

A card reader/punch and printer could be connected to the MTCU to read cards and store them directly on tape or to punch data from tape directly to a card punch or printer. This allowed slow speed I/O operations to be performed in parallel with the 701 ACU.

While investigating magnetic tape storage, IBM built an experimental computer called the Tape Processing Machine. It demonstrated the stability of 7-track magnetic tape. As a result, IBM decided to support 7-track tape, with 6 data tracks and one parity track. This became a near-universal standard for the next two decades.

1.1.9 IBM 740 CRT Recorder Unit

The IBM 740 CRT Recorder Unit provided a pair of CRTs that displayed data presented by programs running in the 701 ACU. The larger tube, 21 inches across, was used for visual display. The CRT had a spot persistence of 20 seconds. The smaller tube was attached to a camera which could photograph the display. It had a persistence of several seconds. Points and alphanumeric characters could be displayed on the CRTs. Under program control, the operator could display stages of a computation and record them via the camera. One point could be displayed every 1.25 microseconds subject to program execution.

1.2 IBM 701 Instruction Set

An IBM 701 instruction was 18 bits long as depicted in Figure 1-4. Thus, two instructions were packed into one 36-bit word. For small memory machines, this allowed larger programs to be stored in memory, but with an increase in the processor's internal complexity to unpack the instructions prior to execution.

Figure 1-4. IBM 701 Instruction Format
Source: Adapted from IBM 1953c, Buchholz 1953

Memory was addressed to the half-word, so the architecture allowed up to 2,048 words. The sign bit of each instruction determined whether the instruction was being used to address words or half-words. Negative instructions were addressed as words, while positive instructions were addressed as half-words. Half words were packed into words in big-endian order, with odd addresses being used to reference the least significant halves.

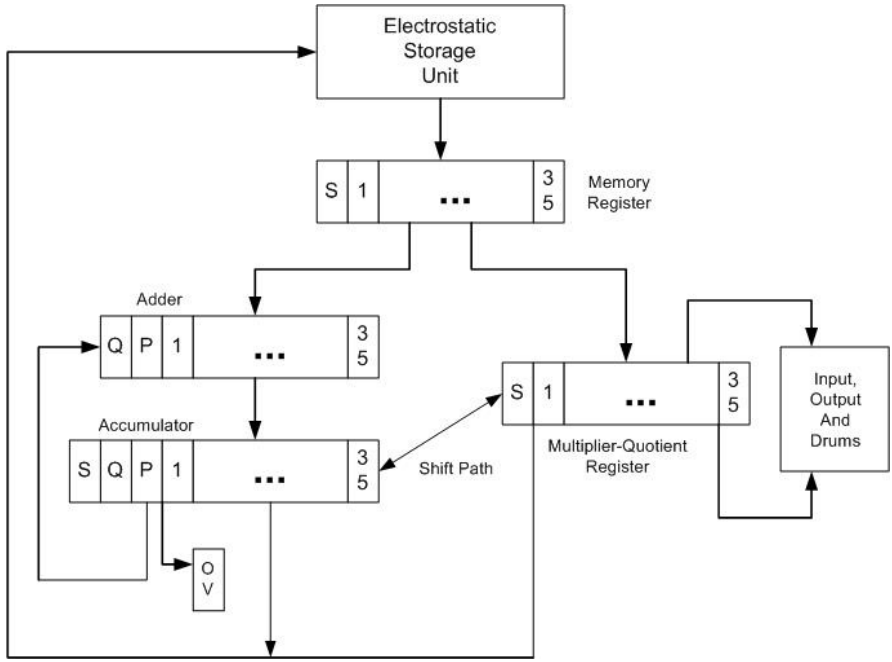

Figure 1-5. IBM 701 Dataflow Paths
Source: Adapted from Buchholz 1953

Given its scientific computing orientation, the IBM 701 had 'round and multiply' and 'round' instructions that incremented the accumulator if the most significant bit of the multiplier-quotient register was one. The data flow path in the IBM 701 is depicted in Figure 1-5. (S – sign bit; OV - overflow indicator; Q, P – overflow positions)

The memory register was not addressable by the program, but was used by the hardware to move data to and from the (ESU. The accumulator and the MQ register were directly addressable by the program. The MQ

register also served as a buffer during certain I/O operations. Thus, it was the only link between the internal memory and the external world as represented by the peripheral devices. Although an instruction might read or write to a memory address, the data was transferred through the MQ register.

Since the sign bit of each instruction determined whether the memory address was a half-word or full-word address, the 5-bit opcode field left room for only 32 instructions. However, the five control flow instructions always addressed half-words, and the four shift instructions and I/O instructions did not use the sign bit. This yielded enough space in the instruction set to extend the machine as later models were introduced. A 33rd instruction was added by using the sign bit for opcode 13 to specify two different instructions.

Table 1-2. IBM 701 Instruction Set

OpCode	Symbolic Form	Description
00	Stop	*Stop and Transfer*: Halted the computer. Transferred to x when the computer was restarted.
01	Tr x	*Transfer*: Retrieved the next instruction from the half-word address x.
02	TrOv x	*Transfer on Overflow*: Transferred to address x if the overflow indicator was on; then reset the overflow indicator.
03	TR+ x	*Transfer on Plus*: Transferred to address x if the accumulator sign was positive.
04	Tr0	*Transfer on Zero*: Transferred to address x if the contents of the accumulator were equal to zero.
05	Sub x	*Subtract*: Subtracted the contents of address x from the accumulator.
06	R Sub x	*Reset and Subtract*: Set the contents of the accumulator to zero before subtracting.
07	Sub Ab x	*Subtract Absolute Value*: Subtracted the absolute value of the contents of address x from the accumulator.
08	NoOp	*No Operation*: CPU fetched the next instruction.
09	Add x	*Add*: Added the contents of address x to the accumulator.

10	R Add x	*Reset and Add*: Set the contents of the accumulator to zero before adding the contents of the electrostatic location x.
11	Add Ab x	*Add Absolute Value*: Added the absolute value of the contents of address x from the accumulator.
12	Store x	*Store*: Stored the contents of the accumulator at address x.
+13	Store A x	*Store Address*: Stored the bit positions 6-17 of the accumulator at the rightmost 12 bits of half-word address x. Note: instruction must have a positive sign.
-13	Extr x	*Extract*: For each accumulator bit that was 0, stored a 0 in the corresponding bit at address x. All other bits were unchanged.
14	Store MQ x	*Store MQ*: Stored the contents of the MQ register at address x.
15	Load MQ x	*Load MQ*: Loaded the MQ register from address x.
16	Mpy x	*Multiply*: Multiply the contents of address x by the contents of the MQ register. The most significant 35 bits are stored in the accumulator and the remaining bits in the MQ register.
17	Mpy R x	*Multiply and Round*: Performed a multiply, then round the contents of the accumulator.
18	Div x	*Divide*: Divided the contents of the accumulator and the MQ register by the contents of address x. The quotient appeared in MQ and the remainder appeared in the accumulator.
19	Round	*Round*: Increased the magnitude of the accumulator by one position if bit 1 of the MQ was 1.
20	L Left x	*Long Left Shift*: Shifted the contents of the accumulator and the MQ register combined left by x places (x <= 255). Set the accumulator sign to that of the MQ register.
21	L Right x	*Long Right Shift*: Shifted the contents of the accumulator and the MQ register combined right by x places (x <= 255). Set the MQ register sign to that of the accumulator.