

# Birth of the Computer



# Birth of the Computer:

*From Drums to Cores*

By

Stephen H. Kaisler

Cambridge  
Scholars  
Publishing



Birthing the Computer: From Drums to Cores

By Stephen H. Kaisler

This book first published 2017

Cambridge Scholars Publishing

Lady Stephenson Library, Newcastle upon Tyne, NE6 2PA, UK

British Library Cataloguing in Publication Data

A catalogue record for this book is available from the British Library

Copyright © 2017 by Stephen H. Kaisler

All rights for this book reserved. No part of this book may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior permission of the copyright owner.

ISBN (10): 1-4438-8511-8

ISBN (13): 978-1-4438-8511-9

This volume is dedicated to my mother, Dolores, and to my wife, Chryl, who have supported this endeavor – each in her own way. Their forbearance allowed me to work on the multiple volumes in this series concurrently. My children, Rebecca and John, both put up with dad's passion for documenting historical computing machines. And, the family cats – Annie, now deceased, and Izzy, Scooby and Tatiana – have all taken turns at sentry duty lying behind my keyboards and ensuring that I worked diligently.



# TABLE OF CONTENTS

List of Figures.....	xvi
List of Tables.....	xix
Acknowledgement.....	xxiii
Introduction .....	xxiv
<b>Part I: Magnetic Drum Machines .....</b>	<b>1</b>
Chapter One.....	3
IBM 650 Magnetic Drum Calculator	
1.1 650 System Architecture.....	4
1.1.1 Magnetic Drum Memory.....	5
1.1.2 Arithmetic Unit .....	7
1.1.3 IBM 650 Self-Checking .....	8
1.1.4 IBM 650 Console .....	10
1.1.5 Magnetic Tape Units .....	11
1.1.6 IBM 652 Control Unit.....	11
1.1.7 IBM 653 High-Speed Core Storage Unit .....	11
1.1.8 IBM 407 Accounting Machine.....	12
1.2 IBM 650 Instruction Set.....	12
1.2.1 I/O Instructions.....	13
1.2.2 Arithmetic Instructions.....	13
1.2.3 Shifting Instructions .....	15
1.2.4 Branching Instructions .....	15
1.2.5 Table Lookup Instruction .....	16
1.2.6 Miscellaneous Instructions.....	16
1.2.7 Index Accumulator Instructions .....	17
1.2.8 Index Accumulator Operations Instructions.....	17
1.2.9 Floating Point Instructions .....	18
1.2.10 IAS Instruction .....	19
1.3 IBM 650 Programming.....	20
1.4 Symbolic Assembly .....	21
1.5 IBM 650 RAMAC .....	22
1.6 IBM 650 Assessment .....	23

Chapter Two .....	25
Royal McBee/Librascope Machines .....	
2.1 LGP-30 System Architecture .....	27
2.2 LGP-30 Instruction Set .....	28
2.3 The Story of Mel .....	30
2.4 LGP-30 Assessment .....	34
2.5 The LGP-21 .....	34
2.5.1 LGP-21 System .....	35
2.5.2 LGP-21 Memory .....	36
2.5.3 LGP-21 Control Registers .....	37
2.6 LGP-21 Instruction Set .....	39
2.7 Timing and Optimization .....	41
2.8 LGP-21 Assessment .....	41
Chapter Three .....	44
Bendix G Machines .....	
3.1 Bendix G-15 .....	44
3.2 G-15 System Configuration .....	50
3.2.1 Short Lines .....	51
3.2.2 Registers .....	51
3.2.3 Command Lines .....	52
3.2.4 I/O System .....	52
3.3 G-15 Instruction Set .....	53
3.3.1 Special Values for S/D Fields .....	54
3.3.2 Special Instructions .....	54
3.4 Peripheral Devices .....	56
3.4.1 Magnetic Tape MTA-2 .....	56
3.4.2 Digital Differential Analyzer DA-1 .....	57
3.4.3 Graph Plotter PA-3 .....	57
3.4.4 Punched Card Coupler CA-1/CA-2 .....	57
3.4.5 Universal Code Accessory AN-1 .....	58
3.5 Programming Languages .....	58
3.5.1 ALGO .....	58
3.5.2 Intercom 1000 .....	61
3.5.3 Sample G-15 Program .....	66
3.6 Tracking Station Application .....	67
3.7 G-15 Assessment .....	68
Further Reading .....	69
Exercises for the Reader .....	70



<b>Part II: Core Memory Machines</b> .....	73
Chapter Four.....	77
RCA BIZMAC I/II	
4.1 BIZMAC System Architecture .....	81
4.2 BIZMAC I/O System.....	83
4.3 Data Representation.....	84
4.4 BIZMAC Instruction Set.....	84
4.5 BIZMAC Assessment .....	85
Chapter Five.....	86
Ferranti Atlas	
5.1 Atlas System Architecture .....	89
5.1.1 Central Processor.....	89
5.1.2 Program Control.....	90
5.1.3 Storage Hierarchy.....	91
5.1.4 Virtual Storage .....	92
5.2 Peripherals .....	94
5.3 Atlas Instruction Set.....	94
5.3.1 Floating Point Arithmetic Instructions .....	96
5.3.2 Indexing Operations .....	97
5.3.3 Atlas Branching Instructions .....	98
5.3.4 Atlas Shifting Instructions.....	99
5.3.5 Atlas Odd/Even test Instructions .....	99
5.3.6 Atlas B-test Register Instructions.....	100
5.3.7 Atlas Instruction Example .....	100
5.4 Atlas Programming .....	101
5.5 The Atlas Supervisor.....	102
5.5.1 Structure of the Atlas Supervisor .....	103
5.5.2 Job Structure.....	105
5.5.3 Programs .....	106
5.5.4 Process Control .....	106
5.5.5 Interrupt Handling.....	107
5.5.6 Atlas Supervisor Assessment .....	108
5.6 Atlas 2.....	108
5.6.1 Atlas 2 Central Processor .....	109
5.6.2 Atlas 2 Memory.....	110
5.6.3 Magnetic Tape.....	112
5.6.4 Magnetic Disc Files.....	113
5.7 The Atlas 2 Supervisor.....	113
5.7.1 Interrupt Routines.....	114

5.7.2 Supervisor Extracode Routines .....	115
5.7.3 Extended Interrupt Routines.....	116
5.7.4 Object Programs .....	116
5.7.5 Error Conditions .....	117
5.8 Atlas Assessment .....	117
Chapter Six .....	120
JOHNNIAC	
6.1 JOHNNIAC System Architecture .....	122
6.2 JOHNNIAC System Configuration .....	123
6.3 JOHNNIAC Instruction Set .....	124
6.3.1 Conditional Transfer Orders.....	124
6.3.2 Transfer Orders .....	125
6.3.3 Add Orders .....	126
6.3.4 Multiply Operations .....	127
6.3.5 Division Orders .....	129
6.3.6 Store Orders.....	130
6.3.7 Register Movement Orders .....	130
6.3.8 Shift Orders .....	131
6.3.9 Input/Output Orders .....	132
6.3.10 Drum Orders.....	133
6.3.11 Logical Product Orders .....	134
6.3.12 Control Orders.....	134
6.4 JOHNNIAC Operation.....	135
6.5 JOSS .....	136
6.5.1 JOSS Structure .....	137
6.5.2 JOSS Remote Console.....	138
6.5.3 JOSS Implementation.....	139
6.6 JOHNNIAC Assessment.....	140
Further Reading .....	141
Exercises for the Reader .....	143
<b>Part III: Transistor Machines .....</b>	<b>145</b>
Chapter Seven.....	147
UNIVAC Solid State Computer	
7.1 Solid State Computer Architecture .....	148
7.1.1 SSC Central Processor.....	152
7.1.2 Magnetic Drum .....	153

7.1.3 Operator's Console.....	154
7.2 SSC80/SSC90 Instructions .....	155
7.2.1 Executing an Instruction.....	156
7.2.2 Arithmetic Instructions.....	156
7.2.3 Transfer Instructions.....	156
7.2.4 Logical and Shift Instructions .....	157
7.2.5 Comparison Instructions.....	157
7.2.6 Translate Instructions .....	158
7.2.7 SS80 Printer Control Instructions.....	158
7.2.8 Card Reader Control Instructions.....	158
7.3 SSC Peripherals .....	159
7.4 Solid State Computer System Software .....	160
7.4.1 FLOW-MATIC .....	160
7.5 SSC Assessment .....	161
Chapter Eight.....	162
UNIVAC 418	
8.1 UNIVAC 418-I .....	163
8.2 UNIVAC 418 System Architecture .....	163
8.3 Instruction Format.....	163
8.3.1 Type I Instructions .....	164
8.3.2 Type II Instructions .....	164
8.3.3 Type III Instructions.....	165
8.4 System Software .....	165
8.5 UNIVAC 418-II.....	165
8.6 UNIVAC 418-III.....	166
8.6.1 UNIVAC 418-III System Architecture.....	167
8.6.2 Command/Arithmetic Unit (CAU).....	168
8.6.3 Main Storage .....	169
8.6.4 I/O Modules (IOMs).....	170
8.6.5 Magnetic Drums .....	173
8.6.6 Attached Processors .....	174
8.6.7 Communications Systems .....	174
8.6.8 Unit Record Peripherals .....	175
8.7 UNIVAC 418 System Software .....	175
8.7.1 RTOS Executive.....	176
8.7.2 Programming Languages.....	181
8.7.3 System Applications.....	182
8.8 UNIVAC 418-III Application .....	183
8.8 UNIVAC 418 Assessment .....	183

Chapter Nine.....	185
UNIVAC 490/494 .....	
9.1 UNIVAC 494.....	187
9.1 System Architecture.....	188
9.1.1 Central Processor.....	189
9.1.2 Memory .....	191
9.1.3 I/O System.....	191
9.1.4 Communications Handling.....	193
9.1.5 Transfer Switch .....	194
9.2 Instruction Set .....	195
9.2.1 Shift Instructions .....	197
9.2.2 UNIVAC 494 Transfer Instructions .....	199
9.2.3 Arithmetic Instructions.....	201
9.3.4 Logical Instructions.....	203
9.3.5 Comparison Instructions.....	204
9.3.6 Jump Instructions .....	205
9.3.7 Sequence Modifying Instructions.....	206
9.3.8 I/O Instructions.....	207
9.3 Peripherals .....	208
9.3.1 Magnetic Drums.....	209
9.3.2 Magnetic Tape Subsystem.....	210
9.3.3 Operator's Console.....	210
9.3.4 High-Speed Printer Subsystem.....	210
9.4 UNIVAC 490/494 System Software.....	211
9.4.1 Primary Input Stream .....	211
9.4.2 Input Cooperative.....	211
9.4.3 Programming Languages.....	212
9.5 UNIVAC 490/494 Assessment .....	212
Chapter Ten .....	214
MIT's TX-0 .....	
10.1 TX-0 System Architecture .....	217
10.1.1 TX-0 Registers .....	217
10.1.2 Toggle Switch Storage .....	218
10.1.3 Main Memory.....	218
10.2 TX-0 Instructions.....	218
10.2.1 TX-0 Operate Instructions.....	219
10.2.2 Combining Instructions .....	220
10.2.3 Modified Instruction Set.....	222
10.3 Operating Modes.....	223
10.4 TX-0 I/O Equipment .....	224

10.5 FLIT .....	224
10.6 TX-1 .....	225
10.7 TX-2 .....	225
10.7.1 TX-2 System Architecture .....	226
10.8 TX-0 and TX-2 Assessment .....	227
Chapter Eleven .....	229
Philco Ford computers	
11.1 Philco 1000 .....	230
11.1.1 Philco 1000 Central Processor .....	231
11.1.2 Philco 1000 System Architecture .....	232
11.1.3 Instruction Set .....	232
11.2 Philco TRANSAC S-2000 .....	233
11.3 TRANSAC S-2000 System Architecture .....	238
11.3.1 Secondary Memory .....	239
11.4 TRANSAC S-2000 Instruction Set .....	240
11.4.1 Program Control .....	241
11.4.2 Instruction Control .....	241
11.4.3 Algorithm Control .....	241
11.4.4 Floating Point Control .....	242
11.4.5 Memory Cycle Control .....	242
11.5 Philco 212 .....	242
11.5.1 Control Unit .....	245
11.5.2 Instruction Unit .....	245
11.5.3 Index Unit .....	246
11.5.4 Arithmetic Unit .....	247
11.5.5 Store Unit .....	248
11.5.6 I/O Subsystem .....	248
11.5.7 Real-Time System .....	249
11.5.8 Philco 212 Instruction Set .....	250
11.6 Operating System 32KSYS .....	265
11.7 TRANSAC S-2000 Software .....	266
11.8 Philco 2400 Input/Output System .....	269
11.8.1 Philco 2400 System Architecture .....	270
11.8.2 Executive Control .....	271
11.8.3 Program Control .....	272
11.8.4 Arithmetic Element .....	273
11.8.5 Main Memory .....	273
11.8.6 Operator Control Panel .....	274
11.8.7 Philco 2400 Instruction Set .....	275
11.8.8 I/O Operations .....	275

11.8.9 Internal Operations .....	279
11.8.10 Arithmetic Operations .....	284
11.8.11 Philco 2400 I/O Devices.....	287
11.9 Assessment of the Philco Machines.....	287
Chapter Twelve .....	289
Bendix G-20 .....	
12.1 Bendix G-20 System Architecture .....	289
12.1.1 Arithmetic Unit .....	292
12.1.2 Registers.....	292
12.1.3 Core Memory .....	293
12.1.4 Interrupts .....	293
12.2 Instruction Set Architecture .....	294
12.2.1 Add/Subtract Operations and Tests .....	294
12.2.2 Logic Operations and Tests .....	296
12.2.3 Repeated Commands.....	297
12.2.4 Multiply/Divide.....	298
12.2.5 Storage Operations .....	298
12.2.6 Index Operations .....	299
12.2.7 Control Operations .....	299
12.2.8 I/O Operations .....	300
12.2.9 Bus Register Operations.....	301
12.3 I/O System .....	302
12.4 G-21 Dual Processor .....	302
12.4.1 G-21 Software .....	303
12.5 Bendix G-20 Assessment .....	303
Chapter Thirteen.....	304
Packard Bell .....	
13.1 PB250 System Architecture .....	306
13.1.1 Central Processor.....	307
13.1.2 Main Memory.....	308
13.1.3 Flexowriter .....	309
13.1.4 Other I/O Devices.....	310
13.1.5 HYCOMP 250.....	310
13.2 PB250 Commands .....	311
13.2.1 Class I Commands.....	312
13.2.2 Class II Commands .....	314
13.2.3 Class III Commands .....	316
13.2.4 Class IV Commands.....	316
13.2.5 Sequence Tag .....	317

13.3 Packard Bell 440 .....	318
13.3.1 PB440 System Architecture .....	321
13.3.2 Memory System .....	322
13.3.3 I/O System.....	323
13.3.4 PB440 Programming .....	324
13.4 PB440 Micro Instruction Format .....	325
13.5 Packard Bell Assessment .....	325
 Further Reading .....	 327
 Exercises for the Reader .....	 328
 Appendix A: Glossary .....	 331
 References .....	 332
 Index .....	 340

# LIST OF FIGURES

- 1-1. IBM 650 Magnetic Drum Computer
- 1-2. IBM 650 System Architecture
- 1-3. IBM 650 Magnetic Drum Assembly
- 1-4. IBM 650 Magnetic Drum Arrangement
- 1-5. IBM 650 Operators Console
- 1-6. IBM 650 Instruction Format
- 1-7. SOAP II Coding Form
  
- 2-1. Royal McBee LGP-30
- 2-2. LGP-30 Instruction Format
- 2-3. LGP-30 Computer System
- 2-4. General Precision LGP-21 Computer System
- 2-5. LGP-21 Brochure
- 2-6. LGP-21 Instruction Format
- 2-7(a). Front of Optimum Address Locator
- 2-7(b) Rear of Optimum Address Locator
  
- 3-1. Bendix G-15 Computer System Advertisement
- 3-2. Bendix G-15 Ad (Datamation 11-60)
- 3-3. Bendix G-15 Advertisement
- 3-4. Bendix G-15 installed at Naval Supersonic Laboratory at MIT
- 3-5. Bendix G-15 with Operator's Console
- 3-6. Bendix G-15 Instruction Format
- 3-7. Simple ALGO Program
- 3-8. Bendix G-15 ALGO Programming Language
  
- 4-1. RCA BIZMAC Used For Military Application
- 4-2. RCA BIZMAC at U.S. Army Tank Automotive Command
- 4-3. RCA BIZMAC II
- 4-4. BIZMAC System Architecture
- 4-5. RCA BIZMAC Instruction Format
  
- 5-1. Manchester University – Atlas 1 Input Area
- 5-2. The Ferranti Atlas Operator Console
- 5-3. Atlas CPU Architecture



- 5-4. Ferranti Atlas One-level Store Concept
- 5-5. Atlas Instruction Format
- 5-6. Central Store Address Structure
- 5-7. Sample Atlas Autocode Program
- 5-8. Structure of the Atlas Supervisor
- 5-9. Titan Computer
  
- 6-1. JOHNNIAC
- 6-2. JOHNNIAC System Architecture
  
- 7-1. UNIVAC Solid State Computer
- 7-2. Univac Solid State Computer Cabinet
- 7-3. UNIVAC SSC90 Voltage Monitoring Panel
- 7-4. UNIVAC SSC90 System Console
- 7-5. UNIVAC SS90 Circuit Board with Ferractors
- 7-6. SSC90 System Architecture
- 7-7. UNIVAC SSC90 Operators Console
- 7-8. SSC80/SSC90 Instruction Format
- 7-9. Jan Lindeboom at the UNIVAC SSC90 Console
  
- 8-1(a). UNIVAC 418 Instruction Format I/II
- 8-1(b). UNIVAC 418 Instruction Format III
- 8-2. UNIVAC 418-II System 12-1. Bendix G-20
- 8-3. UNIVAC 418-III System Configuration
- 8-4. UNIVAC 418 Interrupt Table Pointer Word Format
  
- 9-1. UNIVAC 490
- 9-2. UNIVAC 490 System
- 9-3. UNIVAC 494 System
- 9-4. UNIVAC 494 System Architecture
- 9-5. UNIVAC 404 BCW Format
- 9-6. UNIVAC 494 Cascade System
- 9-7. UNIVAC 494 Instruction Format
  
- 10-1. TX-0 Computer Room
- 10-2. TX-0 at MIT
- 10-3. TX-2 System Architecture
  
- 11-1. Philco 1000 Central Processing Unit Structure
- 11-2. Transac S-1000 Instruction Format
- 11-3. Philco S-2000 Advertisement

- 11-4. Philco Transac S-2000 Advertisement
- 11-5. Philco 210 System
- 11-6. Philco S-2000 Computer System
- 11-7. TRANSAC 2000 Operator Control Panel
- 11-8. TRANSAC S-2000 Repeat Register Format
- 11-9. TRANSAC S-2000 Instruction Address Format
- 11-10. Philco 212 Advertisement
- 11-11. Philco 212 System Configuration
- 11-12. Philco 212 Central Processor
- 11-13. TIO Data Format
- 11-14. Philco 212 Real-Time Order Format
- 11-15. Philco 212 Instruction Format
- 11-16. Philco 212 Address Field Format
- 11-17. DR instruction for Repeating Four Instructions
- 11-18. ALTAC Translation Process
- 11-19. Philco ALTAC Advertisement
- 11-20. Philco 2400 System Architecture
- 11-21. Philco 2400 Operator Control Panel
- 11-22. Philco 2400 Instruction Format
  
- 12-2. Bendix G-20 System Architecture
- 12-3. Bendix G-20 Computer System Advertisement
- 12-4. Bendix G-20 Instruction Format
- 12-5. Repeat Command Instruction Format
- 12-6. Block Transfer Instruction Format
- 12-7. Bendix G-20 Bus Register Layouts
  
- 13-1. Packard Bell 250
- 13-2. Packard Bell 250 Front Panel
- 13-3. Packard Bell 250 System Architecture
- 13-4. PB250 Machine Sector Counter
- 13-5. Flexowriter Console
- 13-6. Packard Bell 250 Command Format
- 13-7. Packard Bell 440
- 13-8. PB440 Operator Console
- 13-9. PB440 Advertisement
- 13-10. Packard-Bell 440 System Architecture
- 13-11. Packard Bell 440 Memory System
- 13-12. Use of a Memory Interchange Unit

# LIST OF TABLES

- 1-1 IBM 650 – Basic Characteristics
- 1-2. Self-Checking Techniques
- 1-3. IBM 650 I/O Instructions
- 1-4. IBM 650 Arithmetic Instructions
- 1-5. IBM 650 Shifting Instructions
- 1-6. IBM 650 Branching Instructions
- 1-7. IBM 650 Table Lookup Instruction
- 1-8 IBM 650 Miscellaneous Instructions
- 1-9. IBM 650 Index Accumulator Instructions
- 1-10. IBM 650 Index Accumulator Instructions
- 1-11. IBM 650 Floating Point Instructions
- 1-12. IBM 650 IAS Timing Ring Instruction
- 1-13. IBM 650 IAS Multiple Word Transfer Instructions
  
- 2-1. LGP-30 Characteristics
- 2-2. LGP-30 Instruction Set
- 2-3. LGP-21 Characteristics
- 2-4. LGP-21 Instruction Set
  
- 3-1. Bendix G-15 Characteristics
- 3-2. Register Roles in Multiplication and Division
- 3-3. Special Values for S/D Fields
- 3-4. Special Instructions
- 3-5. Intercom 1000 Commands
- 3-6. Sample G-15 Intercom 1000 Program to add Two Numbers
- 3-7. Sample G-15 Intercom 1000 Program to compute  $(a^2 - bc)/d$
  
- 4-1. RCA BIZMAC Basic Characteristics
  
- 5-1. Atlas – Basic Characteristics
- 5-2. Floating Point Arithmetic Instructions
  
- 6-1. JOHNNIAC Characteristics (Weik 1961)
- 6-2. Conditional Transfer Orders
- 6-3. Transfer Orders

- 6-4. Add Operations
- 6-5. Multiply Operations
- 6-6. Division Operations
- 6-7. Store and Substitute Operations
- 6-8. Register Movement Operations
- 6-9. Shift Operations
- 6-10. Input/Output Operations
  
- 6-11. Drum Operations
- 6-12. Logical Product Operations
- 6-13. Control Operations
- 6-14. Sample JOSS Program
  
- 7-1. Solid State 80 – Basic Characteristics
- 7-2. SS80 Arithmetic Instructions
- 7-3. SS80 Transfer Instructions
- 7-4. SS80 Logical and Shift Instructions
- 7-5. SS80 Comparison Instructions
- 7-6. SS80 Translate Instructions
- 7-7. SS80 Print Instructions
- 7-8. SS80 Card Reader Instructions
  
- 8-1. UNIVAC 418 Basic Characteristics
- 8-2. UNIVAC 418-III – Basic Characteristics
- 8-3. Magnetic Drum Systems
- 8-4. Mass Storage Systems
  
- 9-1. UNIVAC 490/494 Basic Characteristics
- 9-2. UNIVAC 490/494 Registers
- 9-3. UNIVAC 494 I/O Registers
- 9-4. Special Interpretation of j Designators for Selected Instructions
- 9-5. UNIVAC 494 Shift Instructions
- 9-6. UNIVAC 494 Transfer Instructions
- 9-7. k Field Modification to Enter Bj
- 9-8. UNIVAC 494 Integer Arithmetic Instructions
- 9-9. UNIVAC 494 Floating Point Arithmetic Instructions
- 9-10. UNIVAC 494 Decimal Arithmetic Instructions
- 9-11. Decimal Test Conditions
- 9-12. UNIVAC 494 Logical Instructions
- 9-13. UNIVAC 494 Comparison Instructions
- 9-14. UNIVAC 494 Jump Instructions

- 9-15. UNIVAC 494 Jump Instructions
- 9-16. UNIVAC 494 I/O Instructions
- 9-17. Magnetic Drum Systems
- 9-18. Mass Storage Systems
- 9-19. UNISERVO Magnetic Tape Subsystems
  
- 10-1. TX-0 Basic Characteristics
- 10-2. TX-0 Machine Registers
- 10-3. Operate Instructions
- 10-4. Useful Combinations of Operate Commands
- 10-5. Operating Modes
- 10-6. TX-2 – Basic Characteristics
  
- 11-1. Philco 1000 Basic Characteristics
- 11-2. TRANSAC S-2000 Basic Characteristics
- 11-3. TRANSAC S-2000 Processor Registers
- 11-4. Effective Address Calculation
- 11-5. Philco 212 Addressable Registers
- 11-6. Control Bits for Indirect Addressing
- 11-7. Philco 212 ADD Instructions
- 11-8. Philco 212 SUBTRACT Instructions
- 11-9. Philco 212 MULTIPLY Instructions
- 11-10. Philco 212 DIVIDE Instructions
- 11-11. Philco 212 CLEAR Instructions
- 11-12. Philco 212 TRANSFER Instructions
- 11-13. Philco 212 JUMP Instructions
- 11-14. Philco 212 SHIFT Instructions
- 11-15. Philco 212 INDEX REGISTER Instructions
- 11-16. Philco 212 EXTRACT Instructions
- 11-17. Philco 212 LOGIC Instructions
- 11-18. Philco 212 SPECIAL Instructions
- 11-19. Modifier Interpretation
- 11-20. Magnetic Tape drive Assignments for 32KSYS
- 11-21. Philco 2400 – Basic Characteristics
- 11-22. PCU Registers
- 11-23. Philco 2400 Operator Control Panel Elements
- 11-24. Feed/PUNCH Instructions
- 11-25. MOVE Instructions
- 11-26. Card Punch Instructions
- 11-27. Character Selection Instructions
- 11-28. Printer Instructions

- 11-29. Magnetic Tape Instructions
- 11-30. Setting and Moving Register Values
- 11-31. Moving and Editing Data Instructions
- 11-32. Code Translation Instructions
- 11-33. Field Comparison Instructions
- 11-34. Register Save Instructions
- 11-35. Register Test Instructions
- 11-36. Jump Instructions
- 11-37. Increment and Decrement Instructions
- 11-38. Arithmetic Operations
- 11-39. Philco 2400 Conversion Instructions
- 11-40. Philco 2400 Shift Instructions
- 11-41. Philco 2400 Logical Instructions
  
- 12-1. Bendix G-20 – Basic Characteristics
- 12-2. Bendix G-20 Addressing Modes
- 12-3. Add/Subtract Operations
- 12-4. Arithmetic Test Operations
- 12-5. Logic Operations
- 12-6. Logic Tests
- 12-7. Multiply/Divide
- 12-8. Storage Operations
- 12-9. Index Operations
- 12-10. Transfer Operations
- 12-11. I/O Operations
- 12-12. Block Transfer Operations
- 12-13. Bendix G-20 Bus Registers
- 12-14. Bus Register Operations
  
- 13-1. Packard Bell 250 – Basic Characteristics
- 13-2. PB250 Class I Commands
- 13-3. PB250 Class II Commands
- 13-4. PB250 Class III Commands
- 13-5. PB250 Class IV Commands
- 13-6. Packard Bell 440 – Basic Characteristic

## ACKNOWLEDGEMENT

I wish to acknowledge the staff of Cambridge Scholars Publishing, particularly Sam Baker, the commissioning editor for the series; Ms. Victoria Carruthers, the Author Liaison, and Ms. Sophie Edminson, Design and Coordinator, for shepherding this book from initial manuscript through to publication. I want to acknowledge the diligent and excellent work of my proofreaders, Mrs. Rebecca Williams (daughter) and Mr. Eric Ward, Scouting colleagues. They have made the book immeasurably better through their efforts. Thank you all for help me to make this book a successful publication!

.

# INTRODUCTION

This volume is the second of a multiple volume set on Historical Computing Machines. We continue with the evolution of computing systems from two perspectives. First, a variety of memory systems evolved to provide larger, faster memories. As a consequence, computing machines became more capable and evolved through enhanced functionality. We also see the beginnings of I/O systems which allowed users to interact with the system, and to have persistent storage that was somewhat easier to use for their programs and data.



# **PART I**

## **MAGNETIC DRUM MACHINES**

Pre-core memory machines relied on a variety of devices to provide working memory, including magnetic drums, mercury delay lines, and plated wires. Drum memories were one of the earliest mass storage devices attached to computing machines. Several variations will be addressed in coming chapters as auxiliary storage devices after magnetic disks were developed. Magnetic drums were rotating cylinders whose exterior surfaces were coated with a ferromagnetic material. In most early systems, a linear array of read/write heads was positioned along the length of the drum to store and retrieve bits of data by magnetizing positions on the drum's surface.

Gustav Tauschek, an Austrian national, invented the first magnetic drum in 1932. Early in his career, Tauschek developed several punched card accounting machines. In 1932, he received a US Patent, No. 1880523, entitled "Setting Device for Calculating Machines and the Like", which clearly depicts a rotating drum on which data could be recorded. The patent was received for the magnetic drum. His device could record about 500,000 bits or about 62.5 Kbytes.

The idea of the magnetic drum was further elaborated at the Institute for Advanced Study (IAS) in Princeton, New Jersey in 1946 as a way to provide additional, easily accessible storage for the IAS machine. In the early 1950s, engineers at Engineering Research Associates (ERA) designed and developed a magnetic drum for the main memory of the ERA 1101 (Hill 1950, ERA UNK). Other manufacturers also designed and used their own magnetic drums in 'one-off' designs until the mid-1950s. By then, magnetic drums came into wide use as computer manufacturers developed product lines that needed highly reliable magnetic drum subsystems for main and auxiliary memories for their computers. Reliable, low-cost magnetic drums of varying capacities enabled the production of lower-cost reliable machines.

In its most basic form, a magnetic drum was a cylinder coated with a ferromagnetic material and mounted either vertically or horizontally on a spinning shaft. Most magnetic drums had one head per track. The heads

did not move. The controller selected the head for the track where the data was stored and waited for the data to come under the head. However, the Univac FASTRAND drums had multiple moving heads which reduced cost but increased latency to access and transfer data. As wait time was due solely to the rotational latency of the drum, a number of sophisticated schemes were developed for early machines to optimize the placement of data on the drum. Knowing the time it took to load an instruction or data item from a particular location on the drum, the programmer could place the next sequential data item just at the point where the previous read ended and a new read could begin.

It is interesting to note that the concept of a drum is retained in today's UNIX and variant systems. /dev/drum is used to refer to the default virtual (swap) device. (Gloutnikov UNK)

Part I explores a few of the magnetic drum machines. Others will be described in volumes associated with specific manufacturers, such as National Cash Register (NCR), the Consolidated Engineering Corporation CEC 201, which became Datatron and was bought by Burroughs, and the General Electric GE 210.

**Chapters:**

Chapter One: IBM 650 Magnetic Drum calculator

Chapter Two: Royal McBee/Librascope

Chapter Three: Bendix G computers

## CHAPTER ONE

### IBM 650 MAGNETIC DRUM CALCULATOR

The IBM 650 was IBM's first commercial computer offering. It was a general-purpose, stored-program computer that used a magnetic drum for the primary memory. Hence, it was called the Magnetic Drum Calculator. It evolved from IBM's Card Programmed Calculator (CPC). Frank Hamilton, who designed the ASCC and SSEC, was the designer. Figure 1-1 depicts the IBM 650. The basic characteristics of the IBM 650 are depicted in Table 1-1 (IBM UNKa, Weik 1961).



Figure 1-1. IBM 650 Magnetic Drum Computer

Source: IBM UNKa

Courtesy of International Business Machines Corporation, © International Business Machines Corporation.

**Table 1-1 IBM 650 – Basic Characteristics**

<b>Characteristic</b>	<b>Value/Explanation</b>
Internal Representation	Fixed Point Decimal
# Bits/Word	70 (10 digits of 7 bits each) plus 1 bit for sign
#Instructions/Word	2
# Instructions	42
Instruction Type	Two address: operand and next instruction
CPU Technology	Vacuum Tube
CPU Registers	3 Accumulators – 10 digits (Upper, Lower and Distributor)
Main Memory	Magnetic Core: 60 words Magnetic Drum: Basic: 2,000 words (Model 2); 4,000 words (Model 4) Expanded: up to 10,000 words
Add Time	Fixed Point: 760 microseconds
Multiply Time	Fixed Point: 12 milliseconds
Divide Time	Fixed Point: 16.2 milliseconds

Several thousand of the IBM 650s were delivered beginning in December 1954. This machine's base price was approximately \$182,000. It could also be rented for about \$3,500 per month. At the time, the rental price was about the same as required to rent a fully loaded Cadillac from General Motors.

An academic discount of about 60% made the machine available for \$72,800. For many universities, the IBM 650 was to be their first computer. The academic discount was conditional on the institution teaching computer-related courses. IBM foresaw that a lack of computer professionals would hamper their ability to sell machines into markets that could effectively use them. IBM seeded the programming industry through its academic discount by encouraging the teaching of computer-related courses. The graduates who used IBM computers in their courses were more likely to become buyers of IBM computers when they entered the commercial marketplace.

The last IBM 650 was sold in 1962. However, industry and universities continued to use these workhorse machines for over 10 more years.

## **1.1 650 System Architecture**

The IBM 650 system architecture is depicted in Figure 1-2. The CPU consisted of three units: the accumulator, the distributor, and the adder. All data entering the accumulator first had to pass through the distributor and

the adder. Data going from the accumulator to general drum storage also passed through the distributor.

Arithmetic operations were performed using the contents of the distributor and the contents of the accumulator using the adder which processed data one digit at a time.

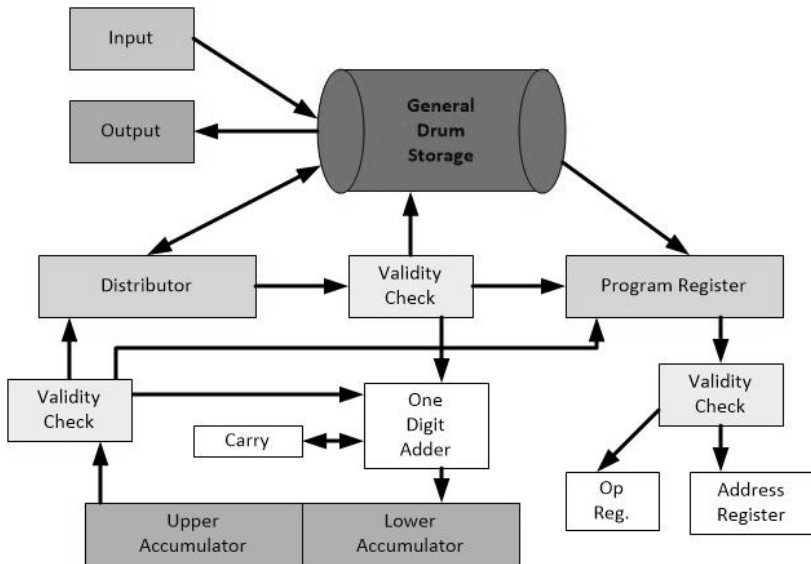


Figure 1-2. IBM 650 System Architecture

Source: Adapted from Andree 1956

### 1.1.1 Magnetic Drum Memory

The IBM 650 primary memory was provided by a magnetic drum, which originally had 1,000 words, then 2,000 words of storage, later expanded to 4,000 words and then, 10,000 words. Figure 1-3 depicts the magnetic drum assembly.

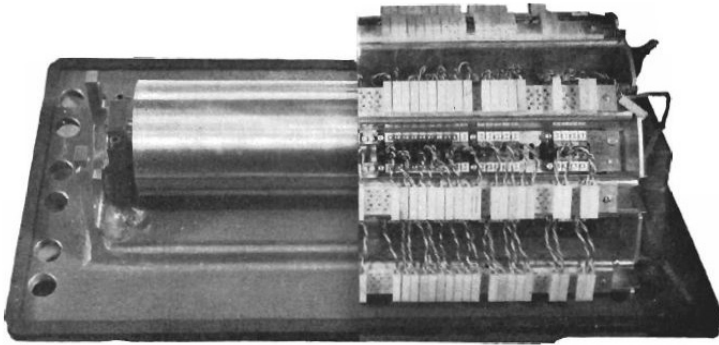


Figure 1-3. IBM 650 Magnetic Drum Assembly

Source: IBM 1957b

Courtesy of International Business Machines Corporation, © International Business Machines Corporation.

The drum had a speed of 12,500 rpm. Parallel to the axis of the drum were attached several inductive heads that read and wrote the information. The general storage portion had 2000 words where ten-digit words could be stored. The word position was location by determining first one of the 40 five-track bands, then determining the angular displacement of the word along the track. Figure 1-4 depicts the layout of the drum.

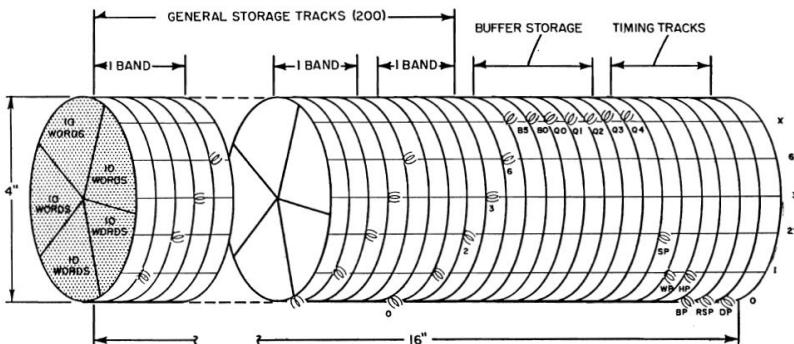


Figure 1-4. IBM 650 Magnetic Drum Arrangement

Source: IBM 1957b

Courtesy of International Business Machines Corporation, © International Business Machines Corporation.